V-3 MICROSTRIP CIRCUITRY FOR INTEGRATED TRANSISTOR AMPLIFIERS

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Experimental and theoretical techniques are described which have been found useful in the development of integrated amplifiers for use at 1.2 Gc/sec and 2.0 Gc/sec.

The three most important design objectives are that these amplifiers shall:

(a) have adequate bandwidth.

(b) be of small dimensions.

(c) have low ohmic losses.

These requirements often conflict and the design is usually a compromise. However, for the RCA developmental transistors which we have used, matching circuits giving 1 dB handwidths of greater than 10% can be attained with combinations of two step transformers and open and shorted stubs.

The choice of values for line impedances is limited by size and attenuation. The characteristics of microstrip line on the 10 mil alumina substrates which we use are shown in Fig. 1. (These are taken from curves[1] calculated from formulae derived by Wheeler[2] and verified experimentally.) It will be seen that values of Z_0 above 50 ohms can be achieved only at the expense of increasing attenuation owing to decreasing line width. It is also advisable to avoid lines of less than 10 ohms to keep size down. The problem of attenuation can be alleviated by using thicker substrates that allow wider lines. However, greater separation between components is then required, and dimensions are increased. Thicker substrates also increase the thermal resistance between the transistor chip and the heatsink on which the substrate is mounted.

Matthaei[3] has given design data for compact impedance transformers using line sections as short as $\lambda/16$. With this data we have been able to construct circuits on alumina substrates having characteristics very close to the given values. Figure 2 illustrates an experiment on 0.010" alumina. Accounting for the edge capacitance in the design yields good agreement with the theory. Thus, in principle, by using shunt stubs at the transistor chips to tune out the associated parallel reactances one can use Matthaei transformers to match the impedance levels. Unfortunately, the power transistors, which we use, require high equivalent shunt load resistances, needing high impedance lines with a large conductor loss with this design method. Nevertheless, the method may find furture application with other transistors or where a series reactance can be inserted, keeping the shunt resistance low.

In practice we have developed a method of computer-aided "cut-and-try" which yields adequate designs. A Fortran computer programme has been written which, given a set of values for the line impedances of a matching network, evaluates the line lengths at the midband frequency and also the conductor attenuation. It is then easy to decide on the best solution for a given problem.

The arithmetic involved in solving a set of transmission line equations and evaluating the loss is considerable and, for an accurate solution, the use of a computer is almost mandatory. However, some generalizations can be made which have been of use in arriving at preliminary configurations which can then be optimised with a computer.

(1) Since short lengths of line can be considered as series inductors or shunt capacitors and shunt stubs as shunt inductors or capacitors, our problem is similar to that of matching transistors with a minimum number of lumped components. This problem has already received attention.[4] The main difference in our case is that we lack the analogue of a high-Q series capacitor.

(2) When a shunt stub is used, in order to get the maximum bandwidth, inductive shorted stubs should have high impedances, capacitative open stubs should have low impedances. This statement is almost obvious, but it highlights the necessity for compromise. Too high an impedance line leads to high losses, too low an impedance to large dimensions.

Table I gives expressions for the conductor loss and bandwidth due to changes in the electrical length of stubs, and also the loss in a one-step transformer. These can be used to evaluate loss and make slide rule approximations of bandwidth.

The first stage in the design of a practical amplifier is the measurement and characterization of the transistor chips. To facilitate this we have developed two types of chip mounts which introduce very little parasitic reactance up to S-band and are easily used in microstrip circuits (Figs. 3 and 4). The transistors are mounted on an alumina microstrip test jig, which is attached to a coaxial system. The transistor is tuned for maximum power gain. The tuning circuits are then removed and their impedances measured to determine the optimum source and load impedances at the position of the transistor. It is important to keep the lengths of microstrip short in order to reduce the effect of their attenuation on the accuracy of the measurements.

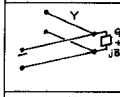
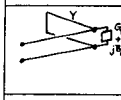
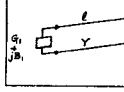
For our prototypes, collector and input bias voltages are fed in through $\lambda/4$ sections of 100 ohm line terminated in a capacitor to ground. In practice we anticipate the use of small chokes to further reduce the area taken up by the decoupling circuitry. (These inductors and their performances are described in a companion paper. It is also expected that, where their low Q is not important, these elements may be used to replace distributed tuning elements.) For stages where the input is at ground potential, a shorted stub may often by used to provide rf matching and dc bias. DC isolation between stages is provided by overlay lines of low impedance deposited over the microstrip lines.

A single-stage 1.2 Gc/sec amplifier is shown in Fig. 5. This has 7.5 dB of gain with 1mW input power over a 1 dB bandwidth of 12.5%. Figure 6 shows gain vs. frequency performance. The transistor chip used is a TA2788 RCA developmental type originally intended for 500 Mc/sec operation. Single- and double-stage 2 Gc/sec power amplifiers have been constructed and will be described.

References

1. M. Caulton, H. Sobol, J.J. Hughes, RCA Review, Vol. 27, pg. 377.
2. H.A. Wheeler, IEEE Trans. on Microwave Theory and Techniques, Vol. 13, pg. 127 (March 1965).
3. G.L. Matthaei, IEEE Trans, on Microwave Theory and Techniques, Vol. 14, pg. 372 (Aug. 1966).
4. G.E. Martes, Electronic Design, July 5, 1966.

TABLE I

	TUNING ELEMENT	INSERTION LOSS / NORMAL ATTENUATION (DB./WAVELENGTH)	FRACTIONAL BANDWIDTH (DB.) DUE TO CHANGE IN ELECTRICAL LENGTH.
	OPEN STUB $+jB$	$\frac{(Y^2+B^2)\ \tan^{-1}\frac{B}{Y}}{4\pi G_1 Y}$	$\frac{4YG\,(Y^2+B^2)}{\left[(Y^2+B^2)^2-4B^2G^2\right]\tan^{-1}\frac{B}{Y}}$
	SHORTED STUB $-jB$	$\frac{(Y^2+B^2)\ \tan^{-1}\frac{Y}{B}}{4\pi G_1 Y}$	$\frac{4GY\,(Y^2+B^2)}{\left[(Y^2+B^2)^2-4B^2G^2\right]\tan^{-1}\frac{Y}{B}}$
SINGLE STEP TRANSFORMER  $\phi=\beta\ell$		INSERTION LOSS / NORMAL ATTENUATION (DB./WAVELENGTH) $=\frac{(G_1^2+B_1^2)(\sin 2\phi+2\phi)+Y^2(2\phi-\sin 2\phi)+2YB_1(1-\cos 2\phi)}{8\pi YG_1}$	

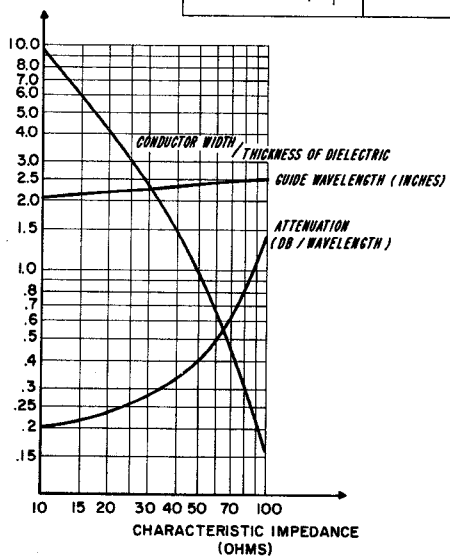


FIG. 1 - Characteristics of Microstrip Lines on 10 MIL. Alumina at 2Gc

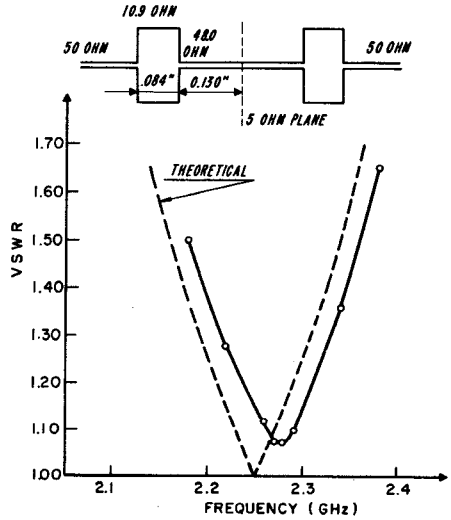


FIG. 2 - Cascade of Two-Section $\lambda/16$ Impedance Transformers Impedance Ratio $1/10$

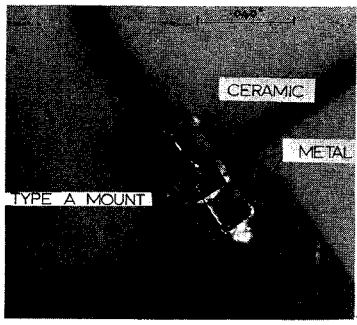


FIG. 3

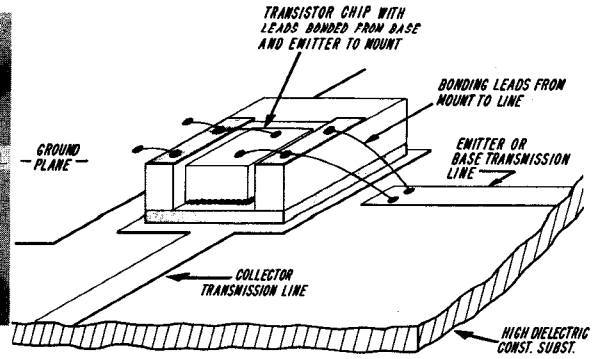


FIG. 4 - Chip Mount for more General Applications

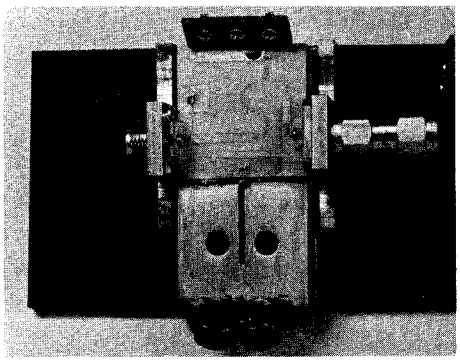


FIG. 5 - 1.2 Gc/sec Amplifier

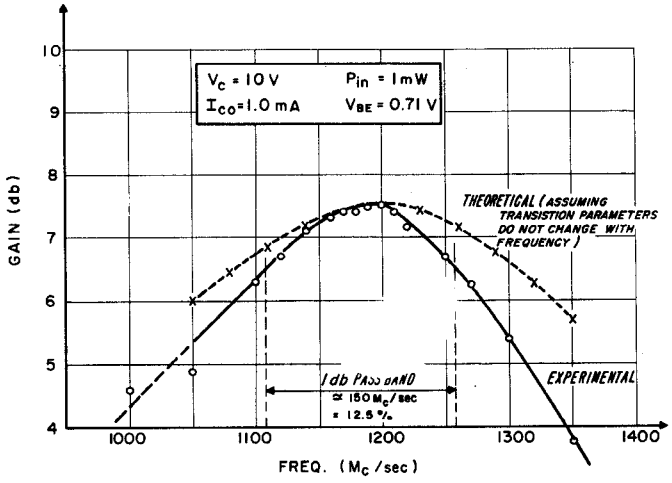


FIG. 6 - Performance of 1.2 Gc/sec Amplifier